We claim:

1. An eventpoint chaining apparatus for generalized event detection and action specification in a processing environment comprising:

a first processing element having a programmable eventpoint module with an input trigger (InTrig) input and two outputs one which produces an OutTrigger (OT) signal and one which produces an EP interrupt signal;

a second processing element having a programmable eventpoint module with an input trigger (InTrig) input and two outputs one which produces an OutTrigger (OT) signal and one which produces an EP interrupt signal, the InTrig input of the second processing element connected to the OT output of the first processing element and the InTrig input of the first processing element connected to the OT output of the second processing element; and

a sequence processor interrupt control unit for receiving processing element EP interrupt signals.

2. The apparatus of claim 1 wherein each of said eventpoint modules further comprises:

means for detecting a generalized processor event (p-event) comprising a change of state it is desirable to recognize; and

means for implementing a generalized processor action (p-action) in acknowledgement in response to the detection of the generalized p-event.

3. The apparatus of claim 1 wherein the first processing element is a sequence processor.

4. The apparatus of claim 1 wherein the first and second processing elements are array processor elements.

5. The apparatus of claim 1 wherein the first and second processing elements both further comprise a special purpose register (SPR) or registers for the storage of the eventpoint parameters.

6. The apparatus of claim 5 wherein eventpoints are separated into two basic classes, instruction eventpoints and data eventpoints and both classes of eventpoints are stored in the SPR file.

7. An eventpoint chaining apparatus for generalized event detection and action specification in a processing environment comprising:

a processing element having at least a first and a second programmable eventpoint module each with an input trigger (InTrig) input and two outputs, one which produces an OutTrigger (OT) signal and one which produces an eventpoint (EP) interrupt signal;

the InTrig of the second eventpoint module connected to the OT output of the first eventpoint module and the InTrig of the first eventpoint module connected to the OT output of the second eventpoint module for the purpose of chaining eventpoints within the processing element.

8. The apparatus of claim 7 wherein the processing element is a sequence processor.

9. The apparatus of claim 7 wherein one eventpoint module is for an instruction eventpoint and the other eventpoint module is for a data eventpoint.

10. The apparatus of claim 7 wherein both eventpoint modules are for instruction eventpoints.

11. The apparatus of claim 7 wherein both eventpoint modules are for data eventpoints.